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Express Mail Label No. EE355009974US

UTILITY PATENT APPLICATION TRANSMITTAL

(Large Entity)

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Docket No.
POU9-2000-0045-US1

JC836 U.S. PTO
09/655595
09/06/00

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.R.F. 1.53(b) is a new utility patent application for an invention entitled:

High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors With Improved Board-to-Board Interconnection Cable Length Identification System

and invented by:

William F. BEAUSOLEIL, R. Bryan COOK, Tak-kwong NG, Helmut ROTH, Peter TANNENBAUM, Lawrence A. THOMAS, and Norton J. TOMASSETTI

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information*:
☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____
Which is a:
☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____
Which is a:
☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 12 pages and including the following:
   a. ☒ Descriptive Title of the Invention
   b. ☒ Cross References to Related Applications (*if applicable*)
   c. ☐ Statement Regarding Federally-sponsored Research/Development (*if applicable*)
   d. ☐ Reference to Microfiche Appendix (*if applicable*)
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings (*if drawings filed*)
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) (Only for new nonprovisional applications under 37 C.F.R. 1.53(b))	Docket No. POU9-2000-0045-US1

Application Elements (Continued)

3. ☒ Drawing(s) (*when necessary as prescribed by 35 USC 113*)

   a. ☐ Formal Number of Sheets _____

   b. ☒ Informal Number of Sheets 2

4. ☒ Oath or Declaration

   a. ☒ Newly executed (*original or copy*) ☐ Unexecuted

   b. ☐ Copy from a prior application (37 CRF 1.63(d)) (*for continuation/divisional application only*)

   c. ☐ With Power of Attorney ☐ Without Power of Attorney

   d. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference (*usable if Box 4b is checked*)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated herein by reference therein.

6. ☐ Computer Program in Microfiche (*Appendix*)

7. ☐ Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all must be included*)

   a. ☐ Paper Copy

   b. ☐ Computer Readable Copy (*identical to computer copy*)

   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers (*cover sheet & document(s)*)

9. ☐ 37 CFR 3.73(B) Statement (*when there is an assignee*)

10. ☐ English Translation Document (*if applicable*)

11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment Postcard

14. ☒ Certificate of Mailing

☐ First Class ☒ Express Mail (*Specify Label No.*): EE355009974US

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) (Only for new nonprovisional applications under 37 C.F.R. 1.53(b))	Docket No. POU9-2000-0045-US1

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (*if foreign priority is claimed*)

16. ☐ Additional Enclosures (*please identify below*):

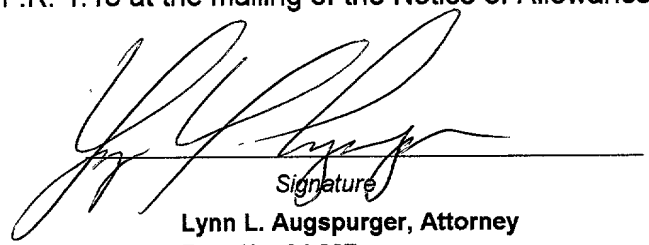
Fee Calculation and Transmittal

CLAIMS AS FILED					
FOR	**#FILED**	**#ALLOWED**	**#EXTRA**	**RATE**	**FEE**
Total Claims	4	- 20 =	0	x $18.00	$0.00
Indep. Claims	1	- 3 =	0	x $ 78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐					$0.00
				BASIC FEE	$690.00
OTHER FEE (*specify purpose*) _____					
				TOTAL FILING FEE	$690.00

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **09-0463** as described below. A duplicate copy of this sheet is enclosed.

- ☒ Charge the amount of $690.00 as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).



Signature

Dated: September 6, 2000

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Docket Number: POU9-2000-0045-US1

HIGH SPEED SOFTWARE DRIVEN EMULATOR COMPRISED OF A PLURALITY OF EMULATION PROCESSORS WITH IMPROVED BOARD-TO-BOARD INTERCONNECTION CABLE LENGTH IDENTIFICATION SYSTEM

APPLICATION FOR

UNITED STATES LETTERS PATENT

"Express Mail" Mailing Label No.:EE355009974US

Date of Deposit: September 6, 2000

I hereby certify that this paper is being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" service under 37 CRF 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Name: Billy R. Stacy

Signature: Billy R. Stacy

Billy R. Stacy

INTERNATIONAL BUSINESS MACHINES CORPORATION

Title: HIGH SPEED SOFTWARE DRIVEN EMULATOR COMPRISED OF A PLURALITY OF EMULATION PROCESSORS WITH IMPROVED BOARD-TO-BOARD INTERCONNECTION CABLE LENGTH IDENTIFICATION SYSTEM

Cross Reference to Related Applications:

The following copending applications, assigned to the assignee of the present invention, contain common disclosure and are incorporated herein by reference in their entireties:

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with an Improved Maintenance Bus that Streams Data at High Speed," Serial No. _____, filed _____, (Attorney Docket No. POU9-2000-0046-US1).

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with a Method to Allow High Speed Bulk Read/Write Operation Synchronous DRAM While Refreshing the Memory," Serial No. _____, filed _____, (Attorney Docket No. POU9-2000-0047-US1).

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with a Method to Allow Memory Read/Writes Without Interrupting the Emulation," Serial No. _____, filed _____, (Attorney Docket No. POU9-2000-0048-US1).

"High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with Improved Multiplexed Data Memory," Serial No. _____, filed _____, (Attorney Docket No. POU9-1999-0183-US1).

Field of the Invention:

The invention relates to software driven emulators comprised of a large number of processors on a module, with a large number of modules on a board, and several boards interconnected by cables of different lengths to comprise the emulator engine. More particularly, the invention relates to a method for determining the cable length used in interconnecting two or more boards.

Trademarks:

S/390 and IBM are registered trademarks of International Business Machines Corporation, Armonk, New York, U.S.A. and Lotus is a registered trademark of its subsidiary Lotus Development Corporation, an independent subsidiary of International Business Machines Corporation, Armonk, NY. Other names may be registered trademarks or product names of International Business Machines Corporation or other companies.

Background:

The usefulness of software driven emulators has increased enormously with growth in the complexity of integrated circuits. Basically, an emulation engine operates to mimic the logical design of a set of one or more integrated circuit chips. The emulation of these chips in terms of their logical design is highly desirable for several reasons. The utilization of emulation engines has also grown up with and around the corresponding utilization of design automation tools for the construction and design of integrated circuit chip devices. In particular, as part of the input for the design automation process, logic descriptions of the desired circuit chip functions are provided. The existence of such software tools for

processing these descriptions in the design process is well suited to the utilization of emulation engines which are electrically configured to duplicate the same logic function that is provided by a design automation tool.

Utilization of emulation devices permits testing and verification via electrical circuits of logic designs before these designs are committed to a so-called "silicon foundry" for manufacture. The input to such foundries is the functional logic description required for the chip and its output is initially a set of photolithography masks which are then used in the manufacture of the desired electrical circuit chip device. Verifying the logic designs are correct in the early stage of chip manufacturing eliminates the need for costly and time-consuming subsequent passes through a silicon foundry.

Another advantage of emulation systems is that they provide a device that makes possible the early validation of software meant to operate the emulated chips. Thus, software can be designed, evaluated and tested well before the time when actual circuit chips become available. Additionally, emulation systems can also operate as simulator-accelerator devices thus providing a high-speed simulation platform.

Emulation engines of the type contemplated by this invention contain an interconnected array of emulation processors (EP). Each emulation processor (hereinafter also sometimes simply referred to as "processor") can be programmed to evaluate logic functions (for example, AND, OR XOR, NOT, NOR, NAND, etc.). The program-driven processors operate together as an interconnected unit, emulating the entire desired logic design. However, as integrated circuit designs grow in size, more emulation

processors are required to accomplish the emulation task. An aim, therefore, is to increase the capacity of emulation engines in order to meet the increasingly difficult task of emulating more and more complex circuits and logic functions by increasing the number of emulation processors in each of its modules.

For purposes of better understanding the structure and operation of emulation devices generally, and this invention particularly, United States Patent No. 5,551,013 and patent application Serial No 09/373,125 filed August 12, 1999, both of which are assigned to the assignee of this application, are hereby incorporated herein by reference. The teachings of the pending application improve the basic design of the 5,551,013 patent by interconnecting processors into clusters.

Patent No. 5,551,013, shows an emulation module having multiple (e.g. 64) processors. Multiple modules are mounted on printed circuit boards, and the boards are interconnected by cables. All processors within the module are identical. The sequencer and the interconnection network occurs only once in a module. The control stores hold a program created by an emulation compiler for a specified processor and the stacks hold data and inputs previously generated, which are addressed by fields in a corresponding control word to locate the bits for input to the logic element. During each step of the sequencer, an emulation processor emulates a logic function according to the emulation program. A data flow control interprets the current control word to route and latch data within the processor. The node-bit-out signal from a specified processor is presented to the interconnection network where it is distributed to each of the multiplexers (one for each processor) of the module. The node address field in the control word allows a specified processor to select for its node-bit-in signal the node-bit-out signal from

any of the processors within its module. The node bit is stored in the input stack on every step. During any operation the node-bit-out signal of a specified processor may be accessed by none, one, or all of the processors within the module.

A bus connected to the processor output multiplexers enables an output from any emulation processor to be transferred to an input of any other of the emulation processors. As explained in the copending application serial number _____, clusters of processors are advantageously interconnected as an emulation engine such that the setup and storing of results is done in parallel, while the output of one evaluation unit is made available as the input of the next evaluation unit. For this purpose, processors share input and data stacks, and have a set of 'cascade' connections which provides access to the intermediate values. By tapping 'intermediate' values from one processor, and feeding them to the next, significant emulation speedup is achieved.

At the operating speeds contemplated for the next generation emulator processor chip (ET4), a signal traveling in an interconnecting cable between two printed circuit boards experiences a propagation delay that must be accounted for in the operation of the system. A number of conductors (e.g. 64) are bundled into each cable, with all conductors in a given cable the same length. Each conductor in the cable is connected at one end to the pin or terminal of an input connector and at its other end to a pin or output terminal. The corresponding input and output pins are identified in a sequential order (e.g. input pin 0 is connected to output pin 0, input pin 1 to output pin 1, and so on). In general, a short cable is desirable because the propagation delay is a function of the cable length. However, because of the physical separation of the various boards that

must be interconnected, it is advantageous to use cables of more than one length; shorter cables where possible and longer cables where necessary. While the propagation delay for a given cable length is known, in a completely assembled emulator engine, the user can not readily determine the length of the cable that has been used. While there have been proposals in the prior art for determining cable lengths in situ, these prior art methods are inefficient.

Summary of the Invention:

An object of this invention is the provision of an efficient system and method for identifying any one of several possible cable lengths in an emulation engine.

Other objects of the invention are a method of cable identification that is automatic, and not susceptible to human error, and efficient, in that actual data conductors are used for the identification; there is no need for dedicated "ID" conductors, which add cost and waste space.

Briefly, this invention contemplates the provision of a system and method for determining which of several possible cable lengths has been used by reversing the end-to-end correspondence of at least two conductors in the cable. A different two conductors are selected to identify respective different cable lengths. Each input pin is connected to a correspondingly identified output pin, except for the pair with the outputs reversed, which pair signifies the cable length. Note that these so-called "board-to-board" cables can be installed such that they start and end on the same board. This improves intra-board processor connectivity.

In operation, a sequence of code signals are coupled to the cable inputs and the corresponding outputs read out. The inverted output pair is detected and this pair identifies the cable length. The operating program is then compiled and the compiled program accounts for the inverted pair as well as the propagation delay generated by a cable whose length is the same as the identified length.

Brief Description of the Drawings:

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention, in which:

Figure 1 is a pictorial diagram illustrating emulator boards of an emulator engine whose outputs and inputs are interconnected by multi-conductor cables of various lengths.

Figure 2 is a pictorial diagram of three cables of different lengths.

Figure 3 is a pictoral diagram illustrating the invention.

Figure 4 is a flow chart of the method steps of determining, in accordance with the teachings of the invention, cable length information in an emulation engine.

Detailed Description of the Invention:

Referring now to Figure 1, as will be appreciated by those skilled in the art, an emulator engine is comprised of a

plurality printed circuit boards 10 to each of which is attached a large number of modules (not shown). Each module includes a large number of processors, as explained in the background section of this application and in the patents and patent applications incorporated herein by reference. Multi-conductor cables 14 are used to interconnect signals from one board to another. It is desirable to keep the cable lengths as short as possible. However, toward achieving this goal, more than one cable length is desirable since a short cable needed to connect certain boards would not be long enough to connect others.

As illustrated in Figure 2, there is a connector 16 (e.g. a pin type connector) on each end of the cable. In the specific exemplary embodiment of the invention, there are sixty-four conductors 15 all of the same length. As will be apparent to one skilled in the art the invention is applicable generally to multi-conductor cables.

Referring now to Figure 3, here the cable has thirty-two "sending" conductors 15 connected to sending pins 00 through 31 of the left-hand connector 16L and connected corresponding receiving pins 00 through 31 of the right-hand connector 16R. It also has thirty-two "receiving" conductors 15 connected to receiving pins 32 through 63 of the left-hand connector 16L and connected to corresponding sending pins 32 through 63 of the right-hand connector 16R. It will be appreciated that the designation sending or receiving to a conductor in cable is not material as far as the cable itself is concerned. With the exception of conductor pairs whose connector pins are interchanged from the pin assignments at one connector relative to the other, the remaining conductors in the cable are "straight through" connections. That is, the individual conductors 15 in the cable connect a pin at one end of the cable to the

corresponding pin at the other end of the cable (e.g. left-hand pin 1 connected to right-hand pin 1, pin 9 connected to pin 9, and so on.).

In order to identify the length of a cable after it has been installed, the end-to-end connections of at least one pair 20 of conductors is swapped. Swapping different pairs denotes different lengths. For example, the shortest cable may have no conductors swapped. The next shortest may have any two consecutively numbered conductors swapped, and the next shortest after that has two other conductors swapped, and so on. Of course, it is not necessary that the swapped pair be consecutively numbered.

In this illustrative embodiment, the conductor connected to the left-hand sending pin 04 is connected to the right-hand receiving pin 05 and the left-hand sending pin 05 is connected to the right-hand receiving pin 04. The emulator is programmed to couple a binary signal to each input pin in a pattern that will allow detection of a swapped pair and the position of the swapped pair in the sequence (e.g. alternating "1s" and "0s").

The emulator stores the received pattern, which can be read out of storage and analyzed in order to identify the swapped conductors and thus to determine the length of cable to which the pattern was coupled. When an emulation program to be run on the emulator is compiled, the various cable lengths that have been determined is inputted to the compiler, which makes the appropriate adjustments in timing to account for the propagation delay through the cable and also makes the appropriate program adjustment so the swapped conductor pair does not cause an error. It will be appreciated that more than one pair may be swapped, if

desired. For example, a pair from the group designated as sending cables and a pair from the group designated as receiving cables.

Referring now to Fig. 4, which summarizes the invention, where the cables of two or more conductor lengths are used to interconnect boards in an emulator engine, at least one pair of receiving pins are physically swapped prior to installation of the cable, block 30. With the cable installed, the emulator is programmed to input a test pattern to the inputs of the cable, block 32. The outputs of the test pattern are collected by the emulator, block 34, and the cable length is determined by detecting the specific swapped pair (or pairs), block 36. The emulation program is compiled for the specific cable length and to account for the swapped output pair or pairs, block 38.

It will also be appreciated that the objects of the invention have been achieved. The method is automatic and not susceptible to human error. The method is also efficient in that actual data conductors are used for identification, so there is no need for dedicated "ID" conductors, which add cost and waste space.

While the preferred embodiment to the invention has been described, it will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for the invention first described.

What is claimed is:

Claim 1. In an emulator that includes printed circuit boards interconnected by a multi-conductor, straight through, cable with inputs at one end of the cable and corresponding outputs at the other cable end, an in situ method for determining the length of the cable, including the steps of:

prior to installing the cable, interchanging the inputs or outputs of at least one pair of conductors to denote a cable length;

programming the emulator to input a test pattern to the cable;

programming the emulator to collect an output data pattern from the cable that results from the test pattern;

determining the cable length from the output pattern;

compiling the emulation program to account for each interchanged pair of conductors.

Claim 2. An in situ method for determining the length of the cable as in claim 1 wherein said test pattern is a pattern of alternating binary "1s" and "0s."

Claim 3. An in situ method for determining the length of the cable as in claim 1 wherein one cable length is denoted by having no interchanged pair of conductors.

Claim 4. An in situ method for determining the length of the cable as in claim 2 wherein one cable length is denoted by having no interchanged pair of conductors.

Title: HIGH SPEED SOFTWARE DRIVEN EMULATOR COMPRISED OF A PLURALITY OF EMULATION PROCESSORS WITH IMPROVED BOARD-TO-BOARD INTERCONNECTION CABLE LENGTH IDENTIFICATION SYSTEM

Abstract:

A system and method for determining which of several possible cable lengths has been used by reversing the end-to-end correspondence of at least two conductors in the cable. A different two conductors are selected to identify respective different cable lengths. Each input pin is connected to a correspondingly identified output pin, except for the pair with the outputs reversed, which pair signifies the cable length.

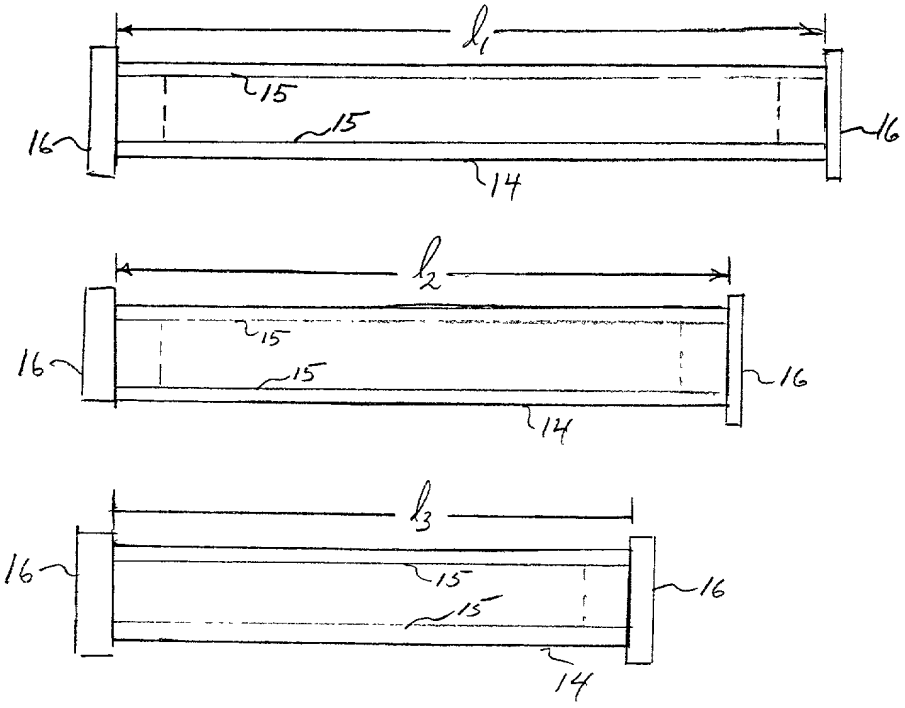
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FIG 2

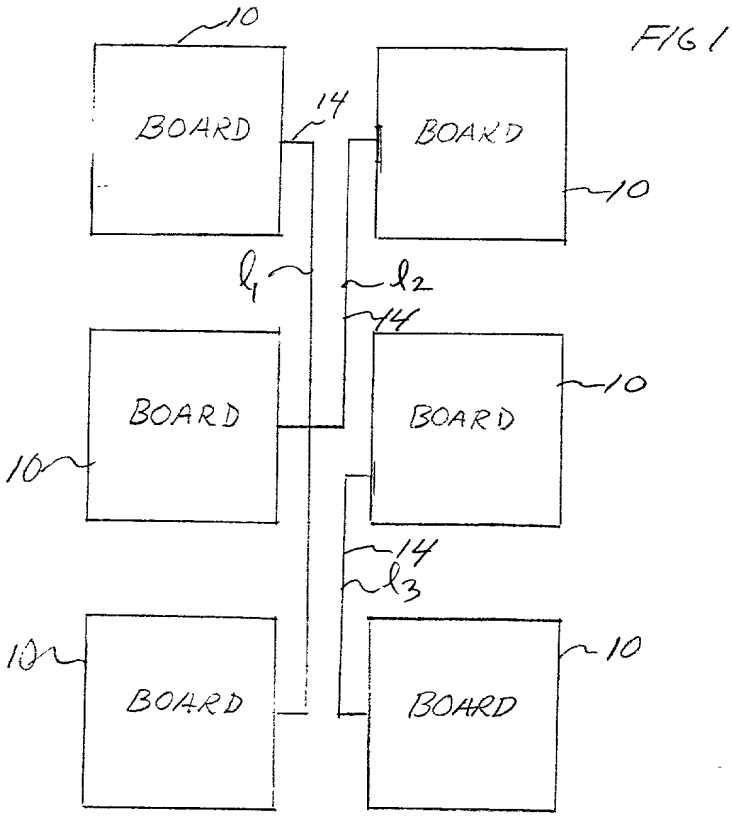
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FIG 1

FIG 3

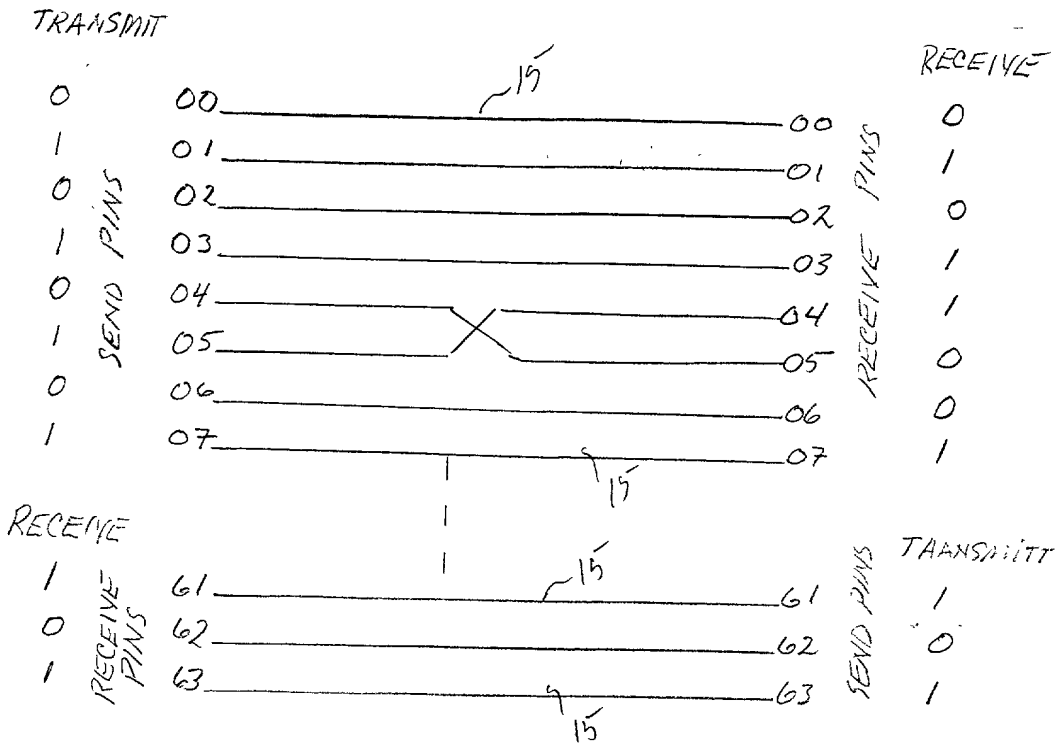
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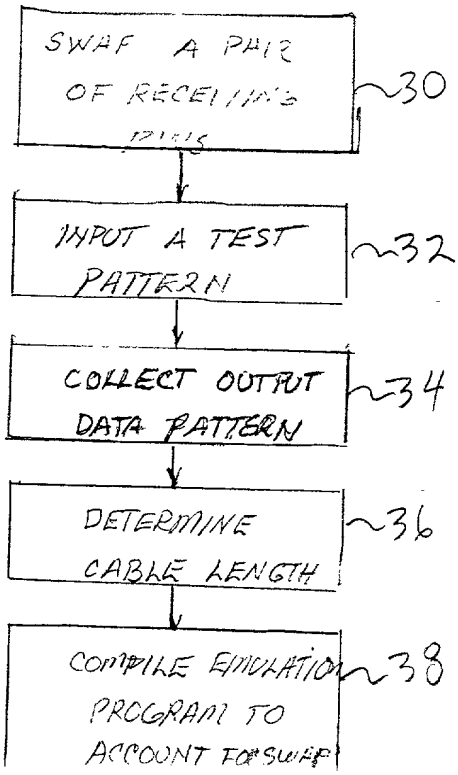
FIG 4


SWAP A PAIR OF RECEIVING PINS
30
INPUT A TEST PATTERN
32
COLLECT OUTPUT DATA PATTERN
34
DETERMINE CABLE LENGTH
36
COMPILE EMULATION PROGRAM TO ACCOUNT FOR SWAP
38

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **HIGH SPEED SOFTWARE DRIVEN EMULATOR COMPRISED OF A PLURALITY OF EMULATION PROCESSORS WITH IMPROVED BOARD-TO-BOARD INTERCONNECTION CABLE LENGTH IDENTIFICATION SYSTEM**

the specification of which (check one)

_X_ is attached hereto
___ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including claims, as amended by any amendment referred to above. I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR Section 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

			Priority Claimed
(Number)	(Country)	(Day/Month/Year Filed)	__ Yes __ No
(Number)	(Country)	(Day/Month/Year Filed)	__ Yes __ No

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under 35 U.S.C Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose material information as defined in 37 CFR Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appl. Serial No.)	(Filing Date)	(Status)(patented, pending, abandoned)
(Appl. Serial No.)	(Filing Date)	(Status)(patented, pending, abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

ADDED PAGE TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR SIGNATURE BY FIRST AND SUBSEQUENT INVENTORS

Lynn L. Augspurger, Reg. No. 24,227; Lawrence D. Cutter, Reg. No. 28,501; Marc A. Ehrlich, Reg. No. 39,966; Floyd A. Gonzalez, Reg. No. 26,732; William A. Kinnaman, Jr., Reg. No. 27,650; Lily Neff, Reg. No. 38,254; William B. Porter, Reg. No. 33,135; Christopher A. Hughes, Reg. No. 26,914; Edward A. Pennington, Reg. No. 32,588; John E. Hoel, Reg. No. 26,279; Joseph C. Redmond, Jr., Reg. No. 18,753; Andrew J. Wojnicki,Jr., Reg. No. 43,995 Richard L. Aitken, Reg. No. 18,791; Clifton E. McCann, Reg. No. 29,565, John P. Shannon, Reg. No. 29,276; Laurence J. Marhoefer, Reg. No. 21,091; Andrew C. Aitken, Reg. No. 36,729; and Ralph P. Albrecht, Reg. No. 43,466.

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Telephone: (202) 962-4800

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: William F Beausoleil Date: 8/31/2000

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Citizenship: United States

Post Office Address: Same as above

Full Name of second joint inventor: ~~Bryan R. COOK~~ R. Bryan Cook (RBC)

Signature: R Bryan Cook Date: 9/5/2000

Residence: 29 Round Hill Road, Poughkeepsie, New York 12603

Citizenship: United States

Post Office Address: Same as above

Full Name of third joint inventor: Tak-kwong NG

Signature: Takkwong Ng Date: 8/31/2000

Residence: 118 Roosevelt Road, Hyde Park, New York 12538

Citizenship: United States

Post Office Address: Same as above

Full Name of fourth joint inventor: Helmut ROTH

Signature: Helmut Roth Date: 9/1/2000

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Citizenship: German

Post Office Address: Same as above

ADDED PAGE TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR SIGNATURE BY FIFTH AND SUBSEQUENT INVENTORS

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Signature: Peter Tannenbaum Date: 8/31/2000

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Citizenship: United States

Post Office Address: P. O. Box 172, Woodstock, New York 12498

Full Name of sixth joint inventor: Lawrence A. THOMAS

Signature: Lawrence A Thomas Date: 9/1/2000

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Citizenship: United States

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